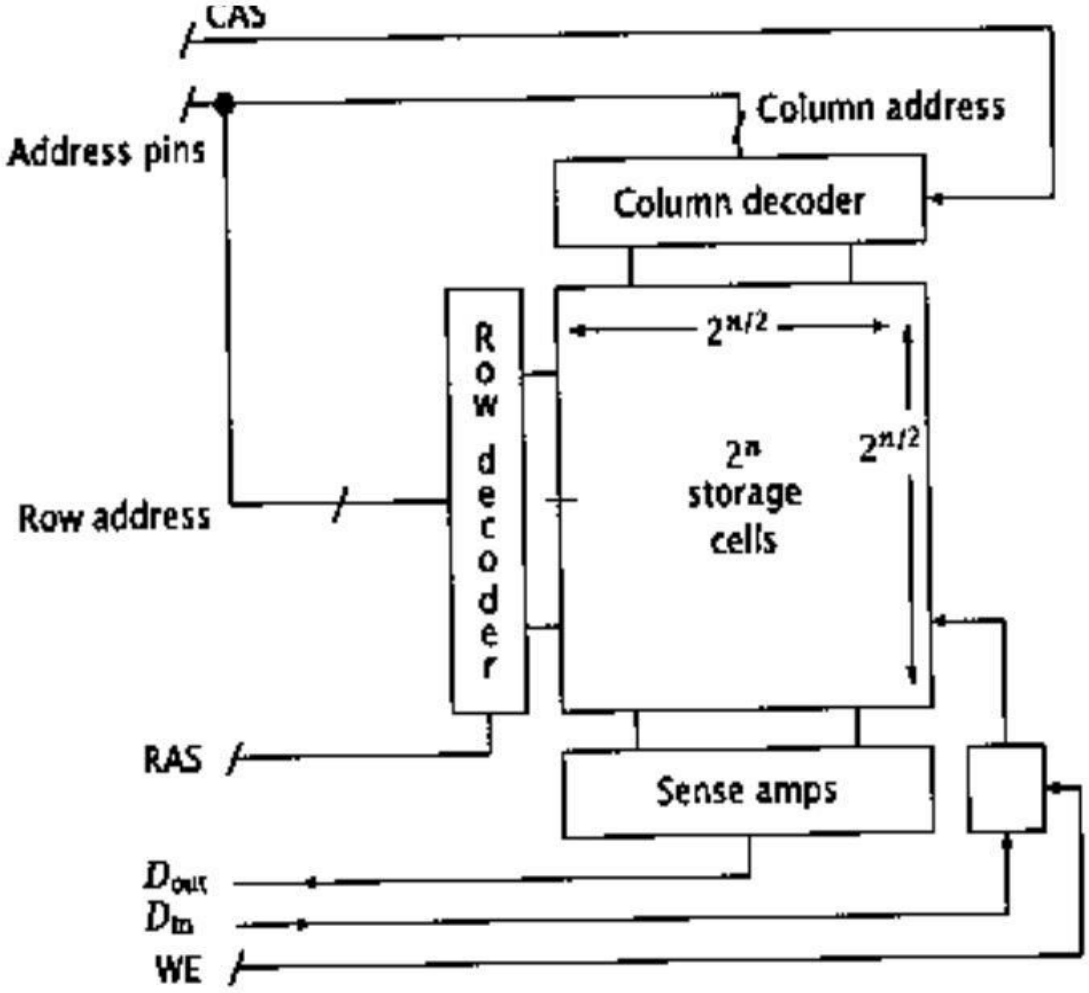
Lecture No 14

Memory Module

Memory Module

- Memory modules are composed of DRAM chips.
- DRAM chip is usually organized as 2^n X 1 bit, where n is an even number.
- Internally chip is a two dimensional array of memory cells consisting of rows and columns.
- Half of memory address is used to specify a row address, (one of $2^{n/2}$ row lines)
- Other half is similarly used to specify one of $2^{n/2}$ column lines.

A Memory Chip



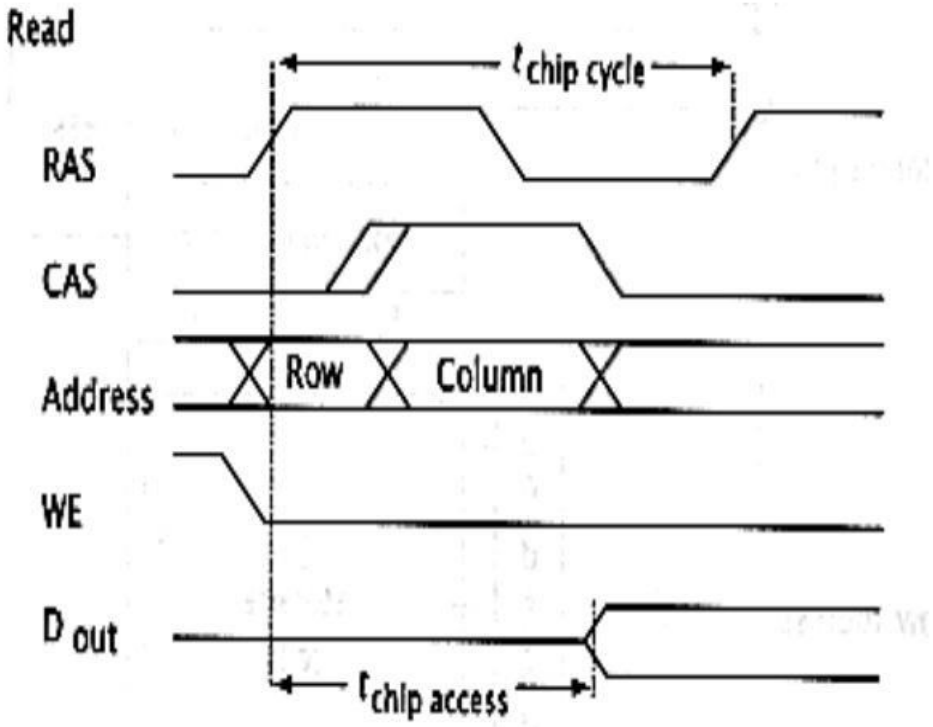
Memory Module

- To save on pinout for better overall density the row and column addresses are multiplexed on the same lines.
- Two additional lines ***RAS*** (Row Address Strobe) and ***CAS*** (Column Address Strobe) gate first the row address and then column address into the chip.
- The row and column address are then decoded to select one out of $2^{n/2}$ possible lines.
- The intersection of active row and column lines is the desired bit of information.

Memory Module

- The column lines signals are then amplified by a sense amplifier and transmitted to the out put pins D_{out} during a *Read Cycle.*
- During a *Write Cycle, the* write enable signal stores the contents on D_{in} at the selected bit address.

Memory Chip Timing



Memory Timing

- At the beginning of Read Cycle, RAS line is activated first and row address is put on address lines.
- With RAS active and CAS inactive the information is stored in row address register.
- This activates the row decoder and selects row line in memory array.
- Next CAS is activated and column address put on address lines.

Memory Timing

- CAS gates the column address into column address register.
- The column address decoder then selects a column line .
- Desired data bit lies at the intersection of active row and column address lines.
- During a Read Cycle the Write Enable is inactive (low) and the output line D_{out} is at high impedance state until its activated high or low depending on contents of selected location.

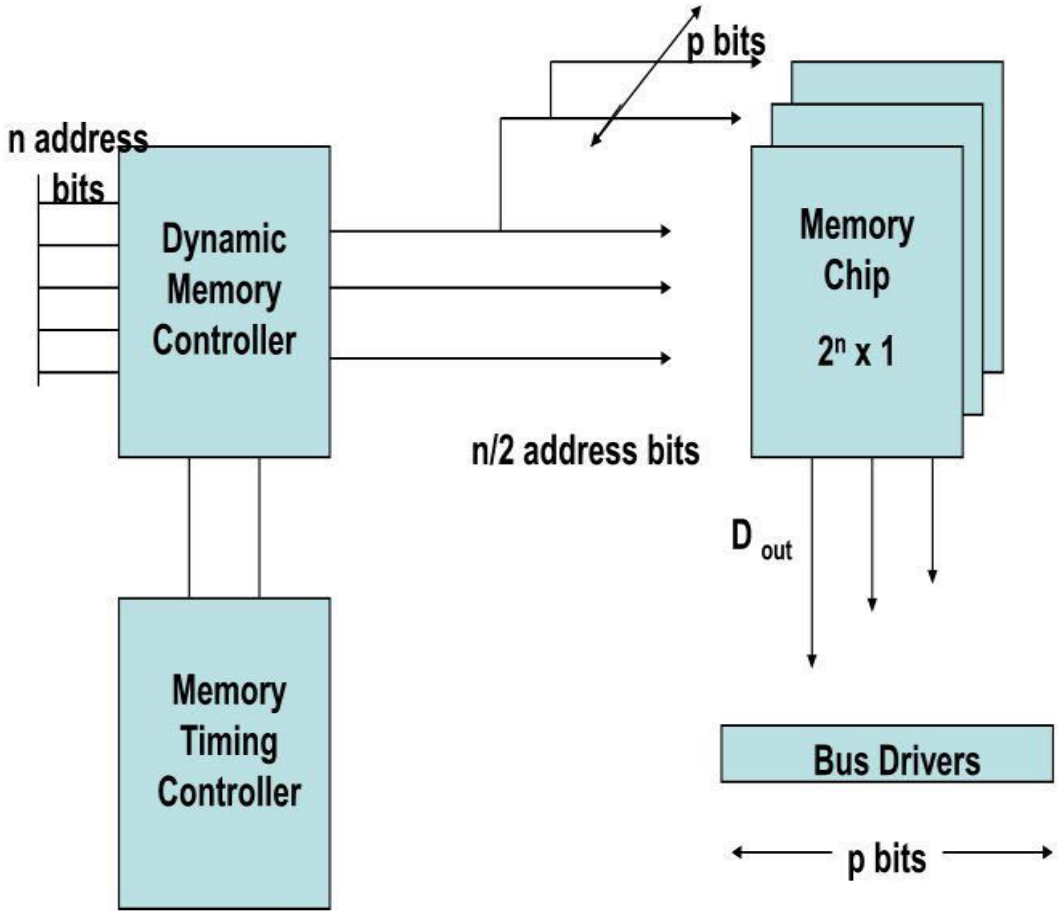
Memory Timing

- Time from beginning of RAS until the data output line is activated is called the chip access time. ($t_{\text{chip access}}$).
- $T_{\text{chip cycle}}$ is the time required by the row and column address lines to recover before next address can be entered and read or write process initiated.
- This is determined by the amount of time that RAS line is active and minimum amount of time that RAS must remain inactive to let chip and sense amplifiers to fully recover for next operation.

Memory Module

- In addition to memory chips a memory module consists of a Dynamic Memory Controller and a Memory Timing Controller to provide following functions.
  - Multiplex of n address bits into row and column address.
  - Creation of correct RAS and CAS signal lines at the appropriate time
  - Provide timely refresh to memory system.

Memory Module



Memory Module

- As memory read operation is completed the data out signals are directed at bus drivers which interface with memory bus, common to all the memory modules.
- The access and cycle time of module differ from chip access and cycle times.
- Module access time includes the delays due to dynamic memory controller, chip access time and delay in transitioning through the output bus drivers.

Memory Module

- So in a memory system we have three access and cycle times.
  - Chip access and Chip cycle time
  - Module access and Module Cycle time
  - Memory (System) access and cycle time.

  (Each lower item includes the upper items)

Memory Module

- Two important features found on number of memory chips are used to improve the transfer rates of memory words.
  - Nibble Mode
  - Page Mode

Nibble Mode

- A single address is presented to memory chip and the CAS line is toggled repeatedly.
- Chip interprets this CAS toggling as mod 2^w progression of low order column addresses.
- For w=2, four sequential words can be accessed at a higher rate from the memory chip.

[00] ---[01]----[10]-----[11]

Page Mode

- A single row is selected and non sequential column addresses may be entered at a higher rate by repeatedly activating the CAS line
- Its slower than nibble mode but has greater flexibility in addressing multiple words in a single address page
- Nibble mode usually refers to access of four consecutive words. Chips that feature retrieval of more than four consecutive words call this feature as ***fast page mode***